

1-536 (U.S. Patent)
09/516615
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257	Class	Subclass	ISSUE CLASSIFICATION
296			

PATENT NUMBER

U.S. UTILITY Patent Application

SCANNED *[Signature]* O.I.P.E. PATENT DATE

APPLICATION NO. 09/516615	CONT/PRIOR	CLASS 257	SUBCLASS 296	ART UNIT 2811	EXAMINER <i>[Signature]</i>
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APPLICANTS

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TITLE

Method of fabricating a polysilicon capacitor utilizing fet and bipolar base polysilicon layers

PTO-2040
12/99

ISSUING CLASSIFICATION							
ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	296	257	532				
INTERNATIONAL CLASSIFICATION							
H01L	27/108						
H01L	29/76,94						
H01L	31/119						
H01L	29/00						
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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 3	Figs. Drwg. 9	Print Fig. 1F	Total Claims 7	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date) _____			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	<i>[Signature]</i> CUONG QUANG NGUYEN 10-28-02 (Primary Examiner) (Date)			11-05-02	
				ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<i>[Signature]</i> 11/02 (Legal Instruments Examiner) (Date)			Amount Due \$1280-	Date Paid
ISSUE BATCH NUMBER					

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